LCP1521S/LCP152DEE

ASD
(Application Specific Devices)

PROGRAMMABLE TRANSIENT VOLTAGE SUPPRESSOR FOR SLIC PROTECTION

FEATURES

- Dual programmable transient suppressor
- Wide negative firing voltage range: V_{MGL} = -150 V max.
- Low dynamic switching voltages: V_{FP} and V_{DGL}
- Low gate triggering current: I_{GT} = 5 mA max
- Peak pulse current: I_{PP} = 30 A (10/1000 µs)
- Holding current: I_H = 150 mA min
- Low space consuming package

DESCRIPTION

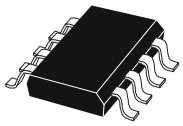
These devices have been especially designed to protect new high voltage, as well as classical SLICs, against transient overvoltages.

Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to $-V_{BAT}$ through the gate.

These components present a very low gate triggering current (I_{GT}) in order to reduce the current consumption on printed circuit board during the firing phase.

BENEFITS

TRISILs™ are not subject to ageing and provide a fail safe mode in short circuit for a better protection. Trisils are used to help equipment to meet various standards such as UL60950, IEC950 / CSA C22.2, UL1459 and FCC part68. Trisils have UL94 V0 resin approved (Trisils are UL497B approved [file: E136224]).



SO-8
LCP1521S

QFN 3x3 6 Leads
LCP152DEE

Table 1: Order Codes

Part Number	Marking
LCP1521S	CP152S
LCP1521SRL	CP152S
LCP152DEERL	LCP

Figure 1: LCP1521S Functional Diagram

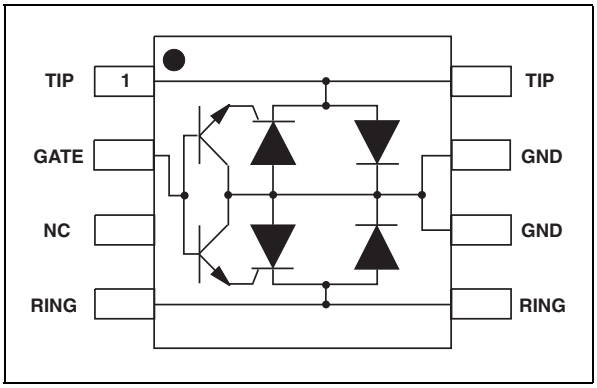


Figure 2: LCP152DEE Functional Diagram

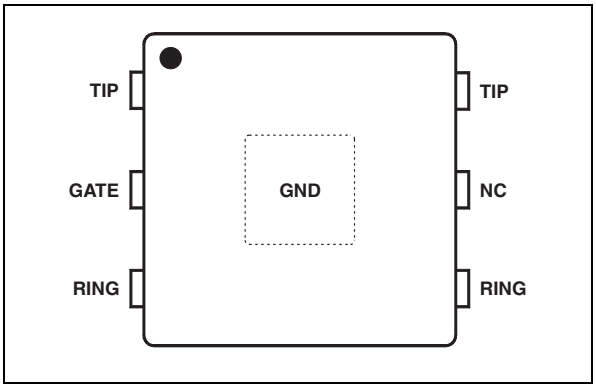


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Table 2: Compliances with the following Standards

STANDARD	Peak Surge Voltage (V)	Voltage Waveform	Required peak current (A)	Current Waveform	Minimum serial resistor to meet standard (Ω)
GR-1089 Core First level	2500 1000	2/10µs 10/1000µs	500 100	2/10µs 10/1000µs	12 24
GR-1089 Core Second level	5000	2/10µs	500	2/10µs	24
GR-1089 Core Intra-building	1500	2/10µs	100	2/10µs	0
ITU-T-K20/K21	6000 1500	10/700µs	150 37.5	5/310µs	110 0
ITU-T-K20 (IEC61000-4-2)	8000 15000	1-60ns	ESD contact discharge ESD air discharge		0 0
VDE0433	4000 2000	10/700µs	100 50	5/310µs	60 10
VDE0878	4000 2000	1.2/50µs	100 50	1/20µs	0 0
IEC61000-4-5	4000 4000	10/700µs 1.2/50µs	100 100	5/310µs 8/20µs	60 0
FCC Part 68, lightning surge type A	1500 800	10/160µs 10/560µs	200 100	10/160µs 10/560µs	22.5 15
FCC Part 68, lightning surge type B	1000	9/720µs	25	5/320µs	0

Table 3: Thermal Resistances

Symbol	Parameter		Value	Unit
$R_{th(j-a)}$	Junction to ambient	SO-8	120	°C/W
		QFN	140	

Table 4: Electrical Characteristics (T_{amb} = 25°C)

Symbol	Parameter
I_{GT}	Gate triggering current
I_H	Holding current
I_{RM}	Reverse leakage current LINE / GND
I_{RG}	Reverse leakage current GATE / LINE
V_{RM}	Reverse voltage LINE / GND
V_{GT}	Gate triggering voltage
V_F	Forward drop voltage LINE / GND
V_{FP}	Peak forward voltage LINE / GND
V_{DGL}	Dynamic switching voltage GATE / LINE
V_{RG}	Reverse voltage GATE / LINE
C	Capacitance LINE / GND

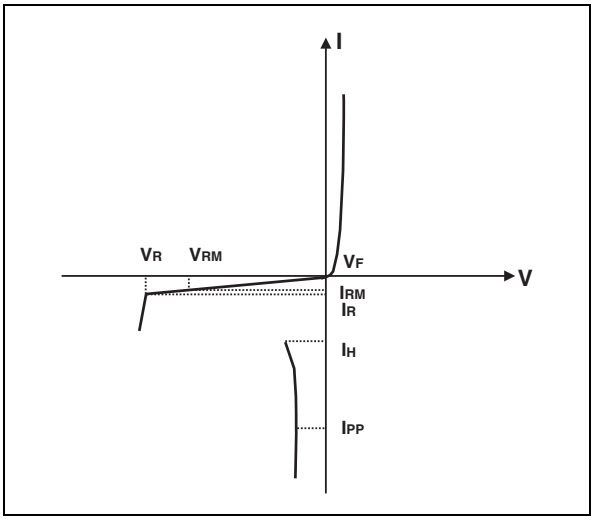


Table 5: Absolute Ratings (T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000µs 8/20µs 10/560µs 5/310µs 10/160µs 1/20µs 2/10µs	30 100 35 40 50 100 150	A
I_{TSM}	Non repetitive surge peak on-state current (50Hz sinusoidal)	t = 20ms t = 200ms t = 1s	12 6 4.5	A
I_{GSM}	Maximum gate current (50Hz sinusoidal)	t = 10ms	2	A
V_{MLG} V_{MGL}	Maximum voltage LINE/GND Maximum voltage GATE/LINE	-40°C < Tamb < +85°C -40°C < Tamb < +85°C	-150 -150	V
T_{stg} T_j	Storage temperature range Maximum junction temperature		-55 to +150 150	°C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

Table 6: Repetitive peak pulse current

Symbol	Definition	Example
t_r	Rise time (µs)	Pulse waveform 10/1000µs: t_r = 10µs t_p = 1000µs
t_p	Pulse duration (µs)	

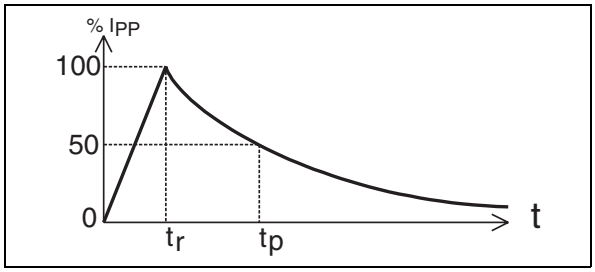


Table 7: Parameters related to the diode LINE / GND (T_{amb} = 25°C)

Symbol	Test conditions			Max	Unit
V_F	I_F = 5A		t = 500µs	3	V
V_{FP} (note 1)	10/700µs 1.2/50µs 2/10µs	1.5kV 1.5kV 2.5kV	R_S = 10Ω R_S = 10Ω R_S = 62Ω	5 9 30	V

Note 1: see test circuit for V_{FP}; R_S is the protection resistor located on the line card.

Table 8: Parameters related to the protection Thyristors (T_{amb} = 25°C, unless otherwise specified)

Symbol	Test conditions			Typ	Max	Unit
I_{GT}	$V_{GND / LINE}$ = -48V			0.1	5	mA
I_H	V_{GATE} = -48V (note 2)			150		mA
V_{GT}	at I_{GT}				2.5	V
I_{RG}	V_{RG} = -150V V_{RG} = -150V		T_j = 25°C T_j = 85°C		5 50	µA
V_{DGL}	V_{GATE} = -48V (note 3)					
	10/700µs 1.2/50µs 2/10µs	1.5kV 1.5kV 2.5kV	R_S = 10Ω R_S = 10Ω R_S = 62Ω	I_{PP} = 30A I_{PP} = 30A I_{PP} = 38A	7 10 25	V

Note 2: see functional holding current (I_H) test circuit

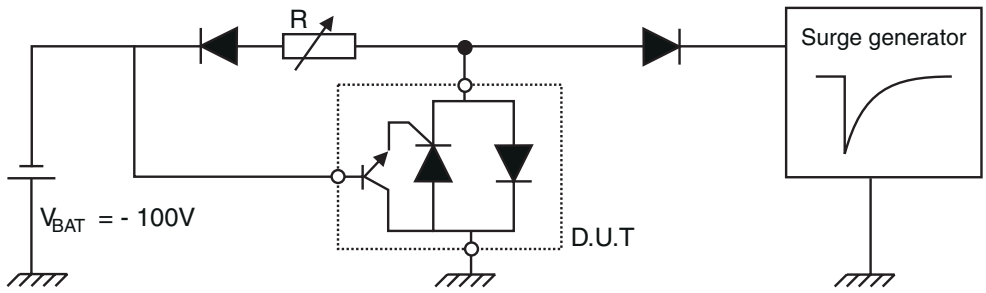
Note 3: see test circuit for V_{DG}

The oscillations with a time duration lower than 50ns are not taken into account.

Table 9: Parameters related to diode and protection Thyristors
(T_{amb} = 25°C, unless otherwise specified)

Symbol	Test conditions		Typ	Max	Unit
I_{RM}	$V_{GATE / LINE}$ = -1V V_{RM} = -150V $VG_{ATE / LINE}$ = -1V V_{RM} = -150V	T_j = 25°C T_j = 85°C		5 50	µA
C	V_R = 50V bias, V_{RMS} = 1V, F = 1MHz V_R = 2V bias, V_{RMS} = 1V, F = 1MHz		15 35		pF

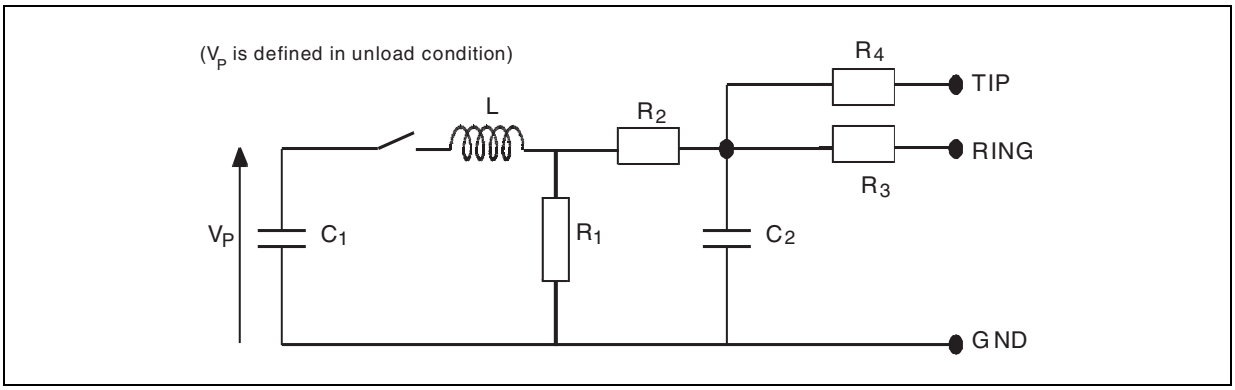
Figure 3: Functional Holding Current (I_H) test circuit: GO-NO GO test



This is a GO-NO GO test which allows to confirm the holding current (I_H) level in a functional test circuit.

TEST PROCEDURE:
- Adjust the current level at the I_H value by short circuiting the D.U.T.
- Fire the D.U.T. with a surge current: I_{PP} = 10A, 10/1000µs
- The D.U.T. will come back to the off-state within a duration of 50ms max.

Figure 4: Test circuit for V_{FP} and V_{DGL} parameters



Pulse (µs)		V_p	C_1	C_2	L	R_1	R_2	R_3	R_4	I_{PP}	R_s
t_r	t_p	(V)	(µF)	(nF)	(µH)	(Ω)	(Ω)	(Ω)	(Ω)	(A)	(Ω)
10	700	1500	20	200	0	50	15	25	25	30	10
1.2	50	1500	1	33	0	76	13	25	25	30	10
2	10	2500	10	0	1.1	1.3	0	3	3	38	62

TECHNICAL INFORMATION

Figure 5: LCP152 concept behavior

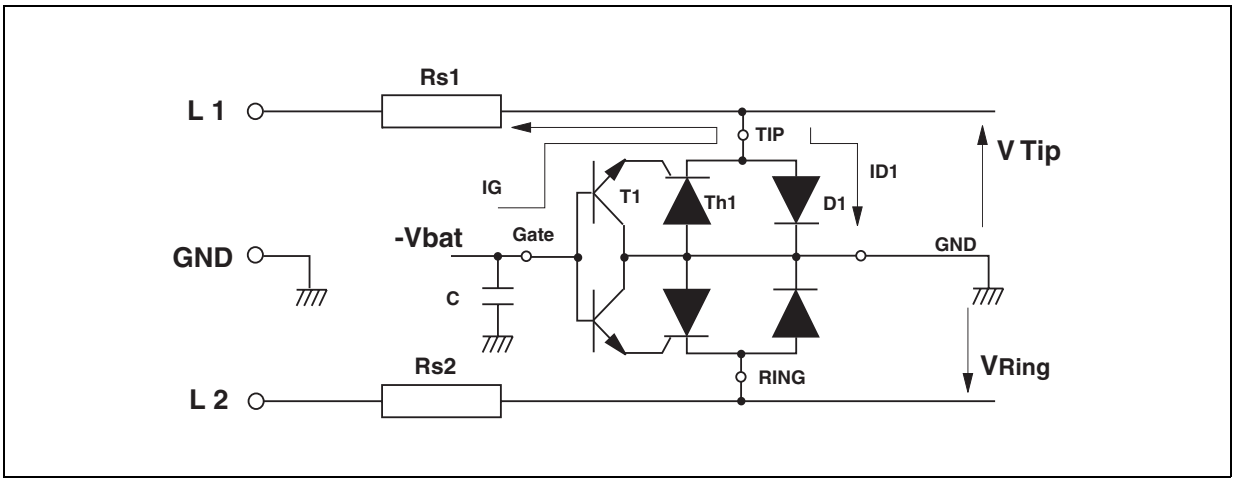


Figure 5 shows the classical protection circuit using the LCP152 crowbar concept. This topology has been developed to protect the new high voltage SLICs. It allows to program the negative firing threshold while the positive clamping value is fixed at GND.

When a negative surge occurs on one wire (L1 for example) a current I_G flows through the base of the transistor T1 and then injects a current in the gate of the thyristor Th1. Th1 fires and all the surge current flows through the ground. After the surge when the current flowing through Th1 becomes less negative than the holding current I_H, then Th1 switches off.

When a positive surge occurs on one wire (L1 for example) the diode D1 conducts and the surge current flows through the ground.

Figure 6: Example of PCB layout based on LCP152 protection

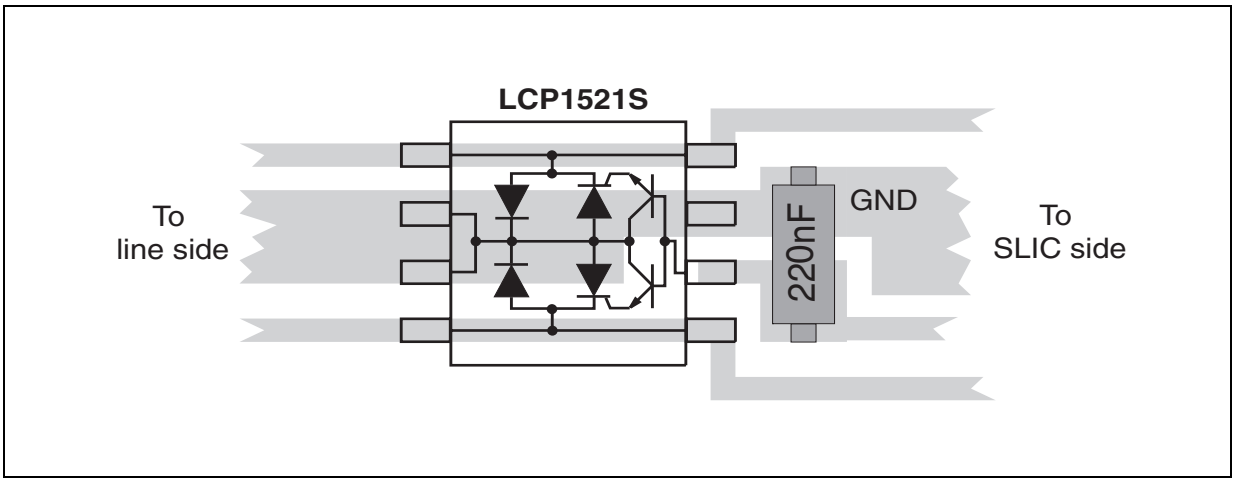


Figure 6 shows the classical PCB layout used to optimize line protection.
The capacitor C is used to speed up the crowbar structure firing during the fast surge edges.
This allows to minimize the dynamical breakover voltage at the SLIC Tip and Ring inputs during fast strikes. Note that this capacitor is generally present around the SLIC - Vbat pin.
So to be efficient it has to be as close as possible from the LCP152 Gate pin and from the reference ground track (or plan) (see figure 6). The optimized value for C is 220nF.

The series resitors Rs1 and Rs2 designed in figure 5 represent the fuse resistors or the PTC which are mandatory to withstand the power contact or the power induction tests imposed by the various country standards. Taking into account this fact the actual lightning surge current flowing through the LCP is equal to:

$$I_{surge} = V_{surge} / (R_g + R_s)$$

With V_{surge} = peak surge voltage imposed by the standard.
R_g = series resistor of the surge generator
R_s = series resistor of the line card (e.g. PTC)

e.g. For a line card with 30Ω of series resistors which has to be qualified under GR1089 Core 1000V 10/1000µs surge, the actual current through the LCP152 is equal to:

$$I_{surge} = 1000 / (10 + 30) = \mathbf{25A}$$

The LCP152 is particularly optimized for the new telecom applications such as the fiber in the loop, the WLL, the remote central office. In this case, the operating voltages are smaller than in the classical system. This makes the high voltage SLICs particularly suitable.
The schematics of figure 7 on next page gives the most frequent topology used for these applications.

Figure 7: Protection of high voltage SLIC

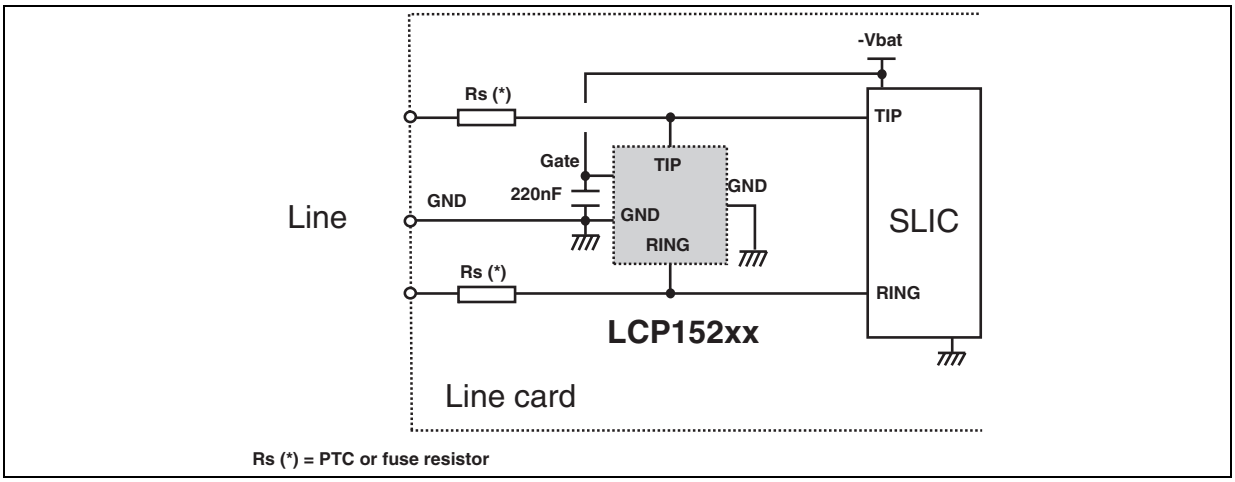


Figure 8: Surge peak current versus overload duration

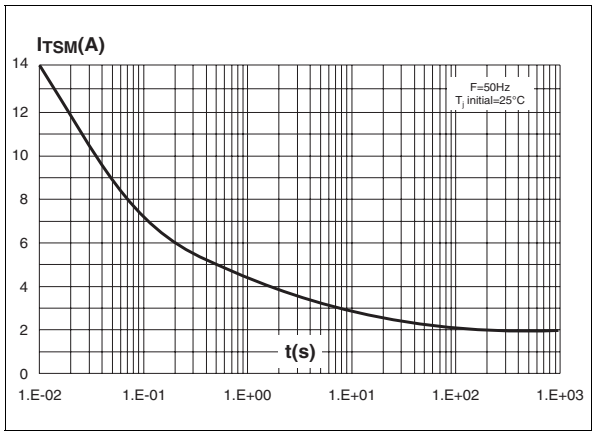


Figure 9: Relative variation of holding current versus junction temperature

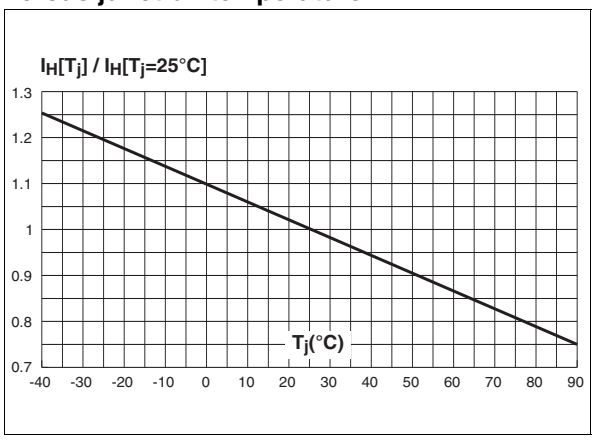
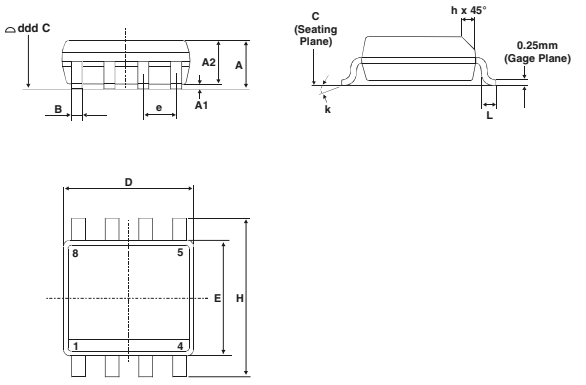


Figure 10: SO-8 Package Mechanical Data



REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.1	0.25	0.004	0.010
A2	1.10	1.65	0.043	0.065
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
e	1.27 Typ.		0.05 Typ.	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.27	0.016	0.050
k	8° (max)			
ddd	0.100		0.004	

Figure 11: Foot Print Dimensions (in millimeters)

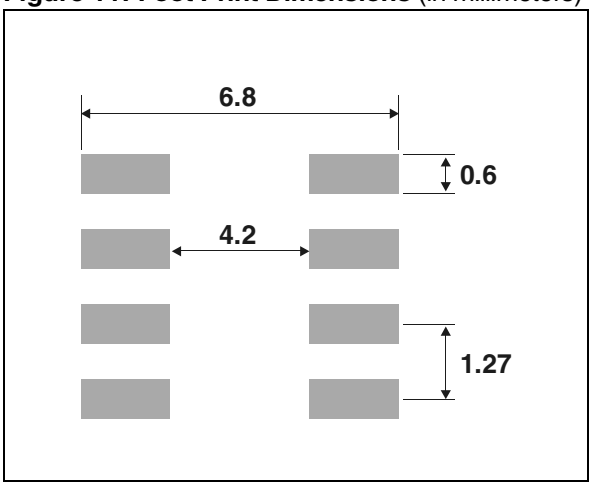
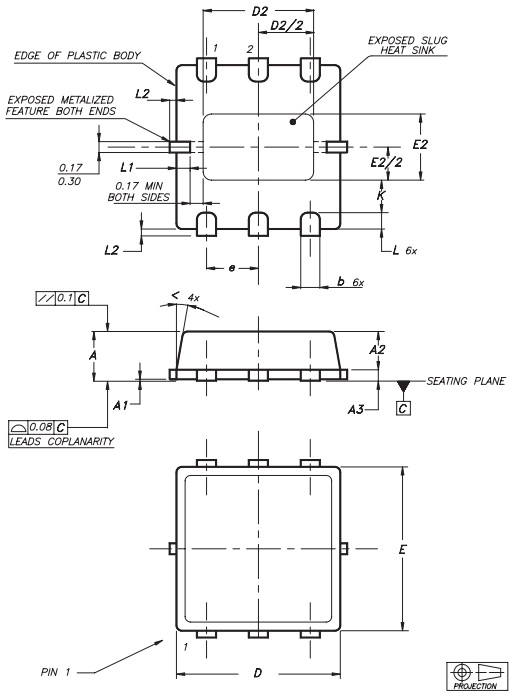


Figure 12: QFN 3x3 S Leads Package Mechanical Data



REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1	0.031		0.040
A1	0		0.05	0		0.002
A2	0.65		0.75	0.026		0.030
A3		20			0.787	
b	0.33		0.43	0.013		0.017
D	2.90	3	3.10	0.114	0.118	0.122
D2	1.92		2.12	0.076		0.083
E	2.90	3	3.10	0.114	0.118	0.122
E2	1.11		1.31	0.044		0.051
e		0.95			0.037	
L	0.20		0.45	0.008		0.018
L1		0.24			0.009	
L2			0.13			0.005
K	0.20			0.008		
<	0°		12°	0°		12°

Figure 13: Foot Print Dimensions (in millimeters)

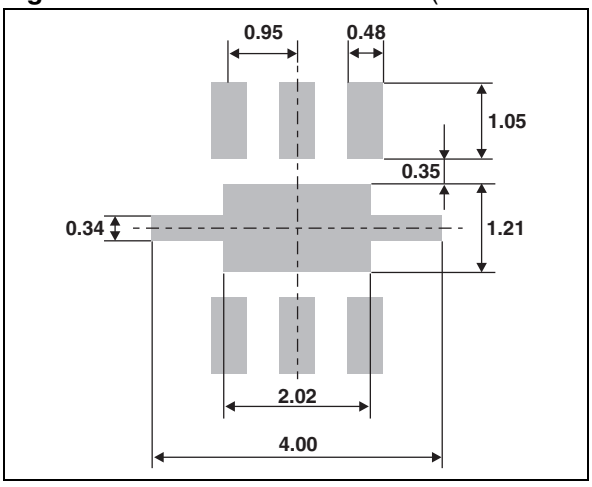


Table 10: Ordering Information

Part Number	Marking	Package	Weight	Base qty	Delivery mode
LCP1521S	CP152S	SO-8	0.08 g	100	Tube
LCP1521SRL	CP152S			2500	Tape & reel
LCP152DEERL	LCP	QFN 3x3 6L	0.022 g	3000	Tape & reel

Table 11: Resision History

Date	Revision	Description of Changes
Sep-2003	1A	First issue.
08-Dec-2004	2	1/ Page 2 table 3: Thermal resistances changed from 130°C/W (SO-8) to 120 °C/W and from 170 °C/W (QFN) to 140°C/W. 2/ SO-8 and QFN footprint dimensions added.
17-Feb-2005	3	Table 9 on page 4: correction of typo on capacitance unit.
03-May-2005	4	Table 5 on page 3: I_{TSM} value @ t= 1s from 4A to 4.5A.